

Article ID: 1007-2780(2010)01-0029-05

Analysis of TFT Array Erosion Defect

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Abstract: There are hundreds of defects happening during TFT-LCD process, especially during array process. Eroded array metal line is one of defects that can cause bright line or thin bright line defect. In this paper, this typical defect was analyzed by SEM, FIB, EDS and statistical software such as BO (Business Objects) and CIM (Computer Integrated Manufacturing). The results show that the defect occurred mainly when the metal layer was eroded by hydrochloric acid gas between Gate Etch process and Multi-Deposition process, and the leakage source of acid gas was identified. The hump in defect position was formed when vacuumizing during Multi-Deposition process. In addition, the emergency measures for this defect were also discussed.

Key words: TFT-LCD; array; failure analysis; erosion

TFT-LCD 阵列腐蚀性缺陷分析

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摘 要: 在 TFT-LCD 的生产过程中, 阵列金属被腐蚀是造成 TFT-LCD 产品缺陷(亮线、薄亮线等)的常见原因。文章对实际生产过程中阵列基板的一种典型腐蚀性缺陷, 应用扫描电子显微镜(SEM)、聚焦离子束(FIB)和能谱仪(EDS)等工具, 并且结合 BO (Business Objects)、CIM (Computer Integrated Manufacturing) 等数据统计软件进行了分析。确定了造成缺陷的原因是栅金属暴露在含氯元素的酸性气体中被腐蚀, 还确定了酸性气体的泄露源, 并且推断出其形成机理: 腐蚀发生在栅金属刻蚀(Gate Etch)工艺和多层膜沉积(Multi-Deposition)工艺之间, 随后的多层膜沉积工艺的抽真空过程促进了缺陷的进一步形成。另外, 针对发生此种缺陷时的应急措施进行了探讨。

关 键 词: TFT-LCD; 阵列; 腐蚀; 缺陷分析; SEM

中国分类号: TN312.8

文献标识码: A

1 Introduction

TFT-LCD is one type of display device addressed by thin film transistor(TFT) active matrix. So the array making process is one of the most important processes for TFT-LCD. It needs 4~6 runs of thin film depositions, photo-

lithography and etching process^[1].

It is a kind of vital defect that metal lines were eroded in array process. The metal lines (gate line, data line and common line) were mainly made of Mo, Cu, and Al or their alloys, etc. Among them, the aluminum alloys prefer to react with most active chemical gas. As a result,

收稿日期: 2009-07-13; 修订日期: 2009-08-10

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the resistance of metal line will become very large to lead to bright line or thin bright line etc. in cell or module^[2,3].

In this paper, this kind of defect was analyzed by SEM, FIB, EDS and some statistic software etc. , such as BO (Business Objects), CIM (Computer Integrated Manufacturing) and so on. The emergency measures for this defect were also discussed.

2 Instruments and Sample

2.1 Instruments

SEM and FIB come from American FEI Company’s Nan lab double beam system Nova 200, Semiconductor material needs vaporizing and plating platinum (Pt) less than 10 nm in thickness. The sample is observed at the accelerating voltage of 10 kV.

EDS spectrum instrument comes from EDAX Company. The spectra of sample can be got from the accelerating voltage of 15 kV during 100 s using the ZAF arithmetic while no referenced sample to qualitative analysis.

FIB incises the sample via the method of physics sputtering to deposit the platinum (Pt) of 300 nm in order to protect the surface of the target sample when the ion beam attacks. The sample was observed with the accelerating voltage of 30 kV and the current of 30 nA. And the depth of the cuneiform incision is large than 2 μm.

2.2 Sample

The sample was the TFT-LCD products with bright line defects. After decapping and

cleaning, the TFT array substrate was observed under the microscope. The array defect was confirmed to be frog egg, and the microscope picture was shown as Fig. 1

3 Results and Discussion

3.1 SEM,EDS & FIB Analysis

It can be confirmed that this defect can lead to gate open or common open by array test^[4]. Under the microscope, it can be seen that the defect distributed on the gate or common line only. In our array process, gate and common line come from the same metal layer. So we think the defect problem belongings to the first metal layer. The further analysis as shown as follows.

From the SEM picture of the defect surface in Fig. 2, it can be seen that these defects are some continuous protuberance. And their shape looks like lots of frog eggs.

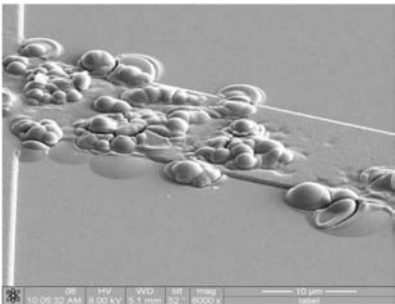


Fig. 2 SEM picture of the defect surface

Fig. 3 is the EDS spectrum of defect surface. It can be seen that the defect surface mainly contains the elements such as N,O,Al,Si,Pt,In,

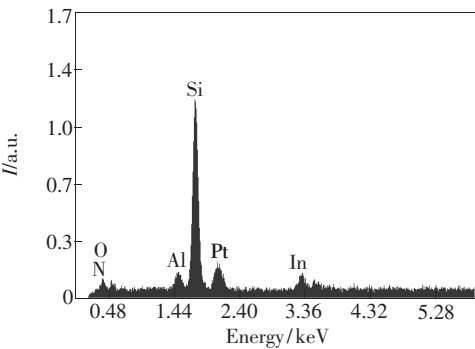


Fig. 3 EDS spectrum of defect surface

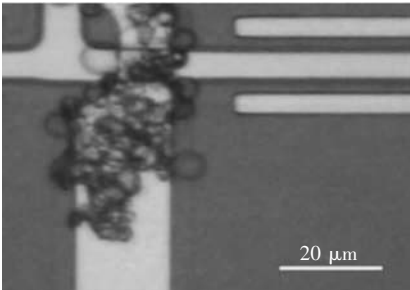


Fig. 1 Microscope picture of the defect area (×100)

etc. And these normal elements come from the gate layer, G-SiN_x gate insulator layer, PVX layer, ITO layer and Pt layer.

The continuous protuberance was split by FIB with the 52° view angle. The picture was shown as Fig. 4. There were too much small holes at the section picture. And there were obvious protuberance on the gate layer. GiN_x layer have the same thickness on the protuberance as normal gate layer. There are the same conclusion with above.

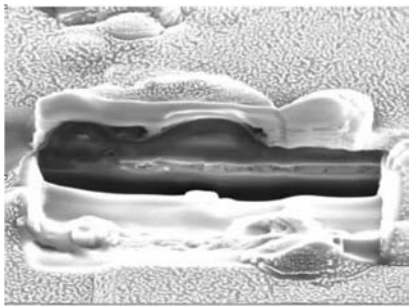


Fig. 4 FIB picture of defect section

From the EDS spectrum of the defect section in Fig. 5, it can be seen that this protuberance is made of O, Al, Si, Cl, etc. element. Cl element is not the ingredient of normal TFT-LCD. But during the array process, the Cl element was only used to dry etch gas as Cl₂ and wet etchant as HCl or other acid.

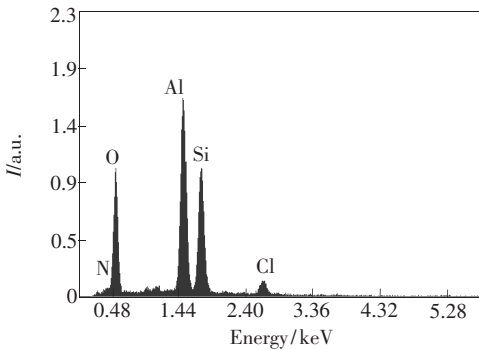


Fig. 5 EDS spectrum of defect section

Gate line was made of two layers: Mo and AlNd. AlNd is so active that it is more easily to be eroded by some active gas or liquid. So the hole appeared at the gate metal layer.

The defect section was observed clearly after dipping for a while in BOE (Buffered Oxide Etchant)solution. From the SEM picture in Fig. 6, it can be seen that the layer distribution: gate metal layer, SiN_x gate insulator layer, active layer, source/drain metal layer and PVX SiN_x layer stacked. The thickness of all layers is normally except that of the gate layer. There are so many holes in the first gate layer. And there is an unknown something existing between the gate layer and GiN_x nonmetal layer. So this defect occurred before the deposition of GiN_x non-metal layer. When these metal layer surface is permeated with the acid gas, the different metal has different electric voltage on their surface. As anode, active Al and Nd lost their electrons in the electrochemistry reaction.

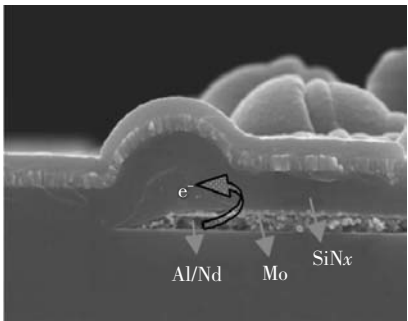
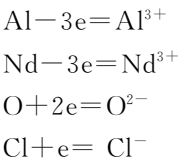


Fig. 6 SEM picture of defect section



When the electrochemical reaction was starting from the anode (Al/Nd), metal Al and Nd transformed to ion state, and interfused to electrolyte or other layer. Then the hole was produced. With the process ongoing, the corroded area spreaded. At last, the Al/Nd/Si/Cl/O compound with very low conductivity was produced. The gate line was influenced by the compounds and the holes. The turn-on voltage is deficient, and resulted in the resistant of gate line becoming higher and higher. At the normal white mode of TFT-LCD, it shows that the bright line

or thin bright line are based on the situation of erosion. The further analysis on process reason of defect was shown as below.

3.2 Process Analysis

At first, all the inspection pictures of this defect panel was traced all through the array process. The earliest defect pictures were found after the same process—Multi-Deposition. The vacuumizing deposition condition of Multi-Deposition lead to the protuberance defects appearing. So we can find it after Multi-Deposition process. On the other hand, all the defects occurred on the gate line or the common line. From the position of the defect, we can conclude that the defects appeared after the forming of gate and common pattern. It is that to say the defect occurred after Gate Etch process.

Secondly, the path of all defect panels was analyzed by CIM (Computer Integrated Manufacturing). We found all the defected panels had

passed through one same position in the same stock equipment between the Gate Etch and Multi-Deposition. The position in the stock equipment and the pipe under the equipment were all checked. A tiny leak was found on the HCl etchant pipe near the equipment.

Lastly, the relevant relation between the defect ratio and delay time which is after Gate Etch process and before Multi-Deposition process was obtained by statistic software BO (Business Object), as in Fig. 7. The defect decreases as delay time goes down, and especially the incidence is very low when delay time is smaller than 300 min. In practical, by means of controlling the delay time less than 300 min, this erosion defect incidence can be very low. As the same time, it is an emergency measure to increase the speed of cycle wind in the product line if this defect appears. But the exactly leakage point have not been found.

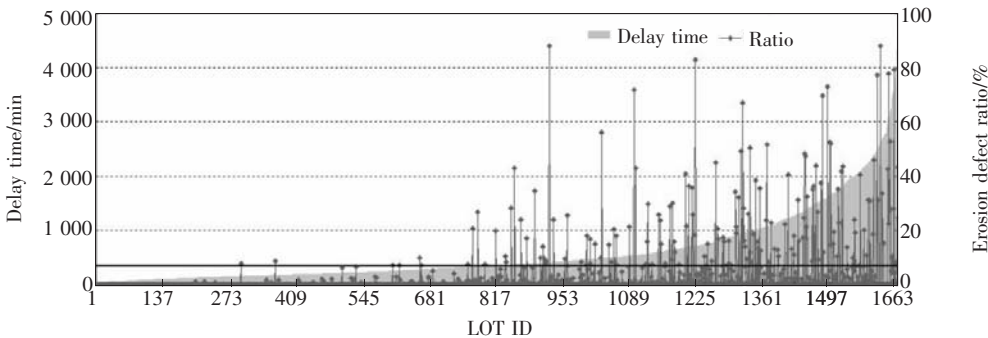


Fig. 7 Relation between erosion defect ratio and delay time

4 Conclusion

This erosion defect results in Gate line or Common line open, which causes vertical bright line or dim bright line in TFT-LCD; In SEM picture, there are so many irregular knotlike protuberance between Gate layer and Gate Insulator layer in FIB section. So judging that the defect formed before Multi-Deposition process, which is caused by erosion of substrate containing Cl element, and the protuberance is caused by vacuum of Multi-Deposition process; By process

analysis and statistic software BO (Business Object), CIM (Computer Integrated Manufacturing), it can be concluded that erosion happened between Gate Etch process and Multi-Deposition process. And by tracking the product process, the leakage position can be confirmed. The reason is HCl enchants leakage; By statistic software, the defect incidence decreases as delay time going down between Gate Etch process and Multi-Deposition process. So when the defect occurred massively, controlling the delay time below 300 min will minimize the loss.

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常见的废弃单位及换算因数

单位名称	符 号	换算因子
英寸	in	1 in=2. 54 cm
托	Torr	1 Torr=133. 322 Pa
毫米汞柱	mmHg	1 mmHg=133. 322 Pa
毫米水柱	mmH ₂ O	1 mmH ₂ O=9. 80665 Pa
西西	cc	1 cc=1 mL
熙提	sb	1 sb=10 ⁴ cd/m ²
尼特	nt	1 nt=1 cd/m ²
屈光度	D	1 D=1 m ⁻¹
体积克分子浓度	M	1 M=1 mol/L
标准大气压	atm	1 atm=101. 325 kPa